

Application No.: 10/064,812

Docket No.: JCLA8774

REMARKSPresent Status of the Application

The Office Action rejected Claims 1-20 under 35 USC 103(a) as being unpatentable over Harrington et al. (US-6,775,192) in view of Miner (US-6,862,704).

After traversing of the aforementioned rejections and amending the claims, Claims 1-21 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of the claim rejection under 35 USC 103(a)

The Office Action rejected Claims 1-20 under 35 USC 103(a) as being unpatentable over Harrington et al. (US-6,775,192, hereinafter "Harrington") in view of Miner (US-6,862,704, hereinafter "Miner").

The following arguments are for the traversing of the rejections of Claims 1 – 20 under 35 USC 103(a) over Harrington in view of Miner.

The Examiner has asserted the following in the Office Action dated October 6, 2005 on page 7 in not accepting the preambles containing "computer main board on/off testing device", "computer main board on/off testing method", or "computer main board on/off testing system" as claim limitations "A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are

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able to stand alone.” The Applicants would like to traverse the rejections under 35 U.S.C. 103(a) in Claims 1-20 based on the following:

FACT 1:

A specific and substantial utility, as described in MPEP 2107, of the present invention required for the compliance of the utility requirements of 35 U.S.C. 101 and 112, first paragraph, described in MPEP 2107, is found specifically with the “computer main board on/off testing device, method, and system”. This is fully supported in Paragraphs [0004]-[0006] of the present invention. In other words, the “computer main board on/off testing device, method, and system” provide for a specific and substantial utility for the on/off testing of the computer main board done automatically and the avoiding of test results deletions due to system failure, as is found in Paragraph [0004]. Therefore, if the “computer main board on/off testing device” is removed from Claims 1-3, for example, as a claim limitation, the remaining features by themselves together in Claims 1-3 as shown below:

command translation unit

test procedure control unit

write-in data display unit

test result display unit

test procedure selection unit

would therefore no longer be able to meet the UTILITY and/or ENABLEMENT requirements (as described in MPEP 2164) for the present invention, and would NOT be able to stand alone (without the “computer main board on/off testing device” as a limiting feature). As one can see that IF SUPPOSE all of the corresponding support such as in paragraphs [0005]-[0006] and in FIG. 1 of

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the present invention for the feature “computer main board on/off testing device” are not accorded any patentable weight, the UTILITY and/or ENABLEMENT requirements of 35 U.S.C. 101 and 112, respectively, would NO longer be met. That is to say the corresponding support in the description used during the claim construction of Claims 1-3 WITHOUT any of the corresponding support dedicated for the feature “computer main board on/off testing device”, as is found, for example, in paragraphs [0005]-[0006] and in FIG. 1, shall no longer be able to support the UTILITY and/or ENABLEMENT requirements.

Therefore, the body of the claim DOES depend on the “computer main board on/off testing device” in the preamble for completeness in Claims 1-3 as well as in Claims 4-8, and the process steps or structural limitations are NOT able to stand alone for the sake of compliance with the UTILITY and/or ENABLEMENT requirements of 35 U.S.C. 101 and 112, respectively.

Furthermore, the body of the Claims 9-14 also depend on the “computer main board on/off testing system” in the preamble for completeness, and the structural limitations are NOT able to stand alone for the sake of compliance with the UTILITY and/or ENABLEMENT requirements of 35 U.S.C. 101 and 112, respectively.

Likewise, the body of the Claims 15-20 depend on the “computer main board on/off testing method” in the preamble for completeness, and the process steps are NOT able to stand alone for the sake of compliance with the UTILITY and/or ENABLEMENT requirements of 35 U.S.C. 101 and 112, respectively.

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FACT 2:

"Any terminology in the preamble that limits the structure of the claimed invention must be treated as a claim limitation" is stated in MPEP 2111.02. As a result, because the "computer main board on/off testing device" is clearly limiting the structure of the claimed invention as shown in FIG. 1, in which the "computer main board on/off testing device 100" and "computer main board on/off testing system" are described. Therefore, the "computer main board on/off testing device" and the "computer main board on/off testing system" are clearly claim limitations in each of their respective claims.

In FIG. 1, It is clearly evident that the TOTAL structure of the claimed "computer main board on/off testing system" comprising the following:

computer main board on/off testing device 100, which includes:

command translation unit 120,

test procedure control unit 130,

write-in data display unit 160,

test result display unit 140, and

test procedure selection unit 150;

computer main board 110, which includes:

PCI interface, and

power switch / reset switch.

Therefore, it is clearly evident that IF the "computer main board on/off testing device 100" were NOT accorded any patentable weight, the remaining features including command translation unit

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120, test procedure control unit 130, write-in data display unit 160, test result display unit 140, and test procedure selection unit 150, AND all of the corresponding support in the disclosure for each of the above remaining claim features (without including "computer main board on/off testing device) would NOT be able to fulfill the written DESCRIPTION requirement under 35 U.S.C. 112, 1st paragraph (as described in MPEP 2163). This is because if the corresponding supporting descriptions found in Paragraphs [0004]-[0006], and [0008] for the "computer main board on/off testing device" and for the "computer main board on/off testing method" were NOT considered in the claim construction for Claims 1-20, the written description requirement under 35 U.S.C. 112, 1st paragraph shall NOT have been met. The subject matter for which protection is sought as defined by the claims as well as all of the corresponding support descriptions in the disclosure WITHOUT the corresponding support descriptions for the computer main board on/off testing device, method, and system would not be able to meet the written description requirement under 35 U.S.C. 112, 1st paragraph because several of the main objectives of the present invention including the on/off testing of the computer main board automatically and the avoiding of test results deletions due to system failure are no longer fully described.

Based on the above traversing, the preambles containing "computer main board on/off testing device", "computer main board on/off testing method", or "computer main board on/off testing system" in Claims 1-20 of the present invention are all clearly **claim limitations** to each of their respective claims. In addition, "computer main board on/off testing device", "computer main board on/off testing method", and "computer main board on/off testing system" are all patentable over Harrington in view of Miner.

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With respect to Claims 1, 13, and 15, the claim limitation “from a specified port address” is neither taught, disclosed, or suggested in Harrington nor Miner. In addition, the Examiner in the Office Action on page 2 did not describe the receiving and translating of data from a specified port address, and no teachings in Miner or Harrington are found for the “receiving and translating of data from a specified port address.” As a result, “from a specified port address” further patentably distinguish Claims 1, 13, and 15 over Harrington in view of Miner.

With respect to Claim 1, 9, 13, 15, and 20, the claim feature “the computer main board” is not taught, suggested, or disclosed in Harrington or Miner. The “computer main board” is NOT an equivalent NOR an obvious variant to the BIST as asserted by the Examiner in the Office Action on page 3, which is found in FIG. 5 of Miner. At best, BIST could only be characterized as a component / feature as part of a “computer main board”. Furthermore, in the present invention, “...computer main board 110 includes a standard interface such as a peripheral component interconnect (PCI) interface, a power on/off switch, a reset switch, a central processing unit (CPU), an advanced configuration & power interface (ACPI) and a basic input/output system (BIOS) such as an Award BIOS (or a Phoenix BIOS)”, which is found in Paragraph [0022], is clearly NOT suggested, taught, or disclosed by the BIST as found in Miner. The “test management logic 570” as included in the citation by the Examiner in the Office Action on page 4 in col. 11, lines 18-20 of Miner, and as shown in FIG. 5 in Miner, is clearly a component of the microprocessor 501, and thus is not an equivalent or obvious variant to the “computer main board” as described above. As a result, the claim feature “computer main board” further patentably distinguish Claims 1, 9, 13, 15, and 20 over Harrington in view of Miner.

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With regard to Claims 4 and 18, the claim feature "on/off test procedure" is not taught, suggested, or disclosed in Harrington or Miner. The Examiner had asserted that a Standby /reduced power state testing is equivalent or obvious to "on/off testing". However, it is impossible to have the device under test to be in an "off" state during either "standby state" or "reduced power state"; for example, US Patent No. 5,241,680 in col. 4, lines 12-14 describes the following: "It should be noted at this point that low-power mode is occasionally referred to herein as "standby"..." Therefore, the "on/off test procedure" is clearly patentable over Harrington in view of Miner. In other words, "on/off test procedure" entails that a device under test is turned on and OFF. Whereas, "standby/reduce power testing" entails that a device under test is NOT turned off (but at a low-power mode instead), and is turned back on at 100% capacity based upon a specific set of rules. As a result, the claim feature "on/off test procedure" further patentably distinguish Claims 4 and 18 over Harrington in view of Miner.

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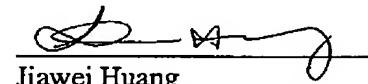
CONCLUSION

For at least the foregoing reasons, it is believed that all the pending Claims 1-21 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date: 1 / 5 / 2006

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809

Respectfully submitted,
J.C. PATENTS


Jiawei Huang
Registration No. 43,330